Amendments to the Drawings

Attached is a replacement drawing of Figure 5 in which reference number 110 has been changed to reference number 510, which replaces the original sheet including Figure 5.

Remarks/Arguments

In this reply, Applicants respectfully offers to amend claims 1, 3, 11, and 21. These amendments do not introduce new subject matter and therefore, do not introduce new issues. Therefore, no new searches are required. Claims 1 and 21 have been further amended to correct informalities.

Specification

The Examiner objected to the specification because of informalities. Accordingly, attached is a replacement drawing of Figure 5 in which reference number 110 has been changed to reference number 510.

Claim Objections

Claims 1 and 21 were objected to because of informalities. Accordingly, claims 1 and 21 have been amended to replace the word "gates" with the word "gate"

Response to Arguments

In the Office Action, the Examiner states, among other things that

> Since claims 1 and 21 in present application, applicant does not provide an NMOS is defined as the write device, and a PMOS is defined as a read device in claim 1. More specifically, in specification page 8, and figures 3 and 5, applicant disclosed a PMOS transistor 305 (TW) is a read device, and an PMOS transistor 110 (TR) is a read device in page 8, lines 5-6, lines 9-10. For these reasons, the applicant's arguments become improperly.
> * Underline added. *See* Office Action, page 3, first paragraph.

Applicants are somewhat puzzled by this statement since page 10, lines 2-9 (with reference to Figure 5) of the specification discloses in an alternative embodiment of the invention, a PMOS device 510 as the read device and an NMOS device 505 as the write device. Applicants therefore submit that claims 1-3, 11-17, and 21-23, are supported by the specification.

Rejections under 35 U.S.C. § 102(b)

In the Office Action, claims 1-3 and 21-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,953,249 to Jan P. Van der Wagt (herein "*Van der Wagt*"). Applicants respectfully request reconsideration of this rejection for at least the following reasons.

In rejecting claim 1, the Examiner alleges that "Van der Wagt discloses a two-transistor DRAM cell (Figure 4) comprising: a NMOS device with a first gate (22); and a PMOS device with a second gate (20), the PMOS device coupled to the NMOS device; and *a storage node (SN) coupled to the second gate (Figure 4, 22)*. . . ." Italics added. Applicants respectfully disagree. In particular, the storage node (SN) of the memory cell device depicted in Figure 4 of *Van der Wagt* is **clearly** shown to be coupled to the first gate of the n-channel FET 22 **instead** of the second gate of the p-channel FET 20. For at least these reasons, claim 1 is patentable over *Van der Wagt*.

Independent claim 21 has similar features as claim 1 and is, therefore, also likewise patentable over *Van der Wagt*. Claims 2-3 and 22-23 depend from and add additional features to independent claims 1 and 21, respectively. Therefore, by virtue of their dependency, claims 2-3 and 22-23 are also patentable over *Van der Wagt*.

In the Office Action, under the heading of "Claim Rejection – 35 USC § 103" on page 4, claims 1-3 and 21-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,010,519 to Yoshimoto et al. ("*Yoshimoto*"). Applicants are somewhat puzzled by this rejection since the Examiner fails to indicate where in *Yoshimoto* are the features of claims 1-3 and 21-23 taught. Further, Applicants were unable to discern where in *Yoshimoto* are any of the features of claims 1-3 and 21-23 taught. If the Examiner chooses to maintain this rejection, then the Applicants respectfully request the Examiner indicate where in *Yoshimoto* are the features of claims 1-3 and 21-23 taught.

Rejections under 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected claims 11-17 under 35 U.S.C. § 103(a) as being unpatentable over *Van der Wagt*, *Yoshimoto* and in further view of

U.S. Patent No. 6,787,835 to Atwood et al. ("*Atwood*"). Applicants respectfully disagree for at least the following reasons.

As currently amended, independent claim 11 now recites, among other things:

> A two-transistor DRAM cell consisting:
> a read bit line;
> a write bit line;
> a read word line;
> a write word line;
> a p-channel (PMOS) device coupled between the read bit line and the read word line; and
> an n-channel (NMOS) device coupled between the write bit line and a gate region of the PMOS device so as to form a storage node therebetween.
>
> * Underline added.

In the Office Action, the Examiner states:

> As described above, and Figure 3 of Yoshimoto et al. disclosed all of elements except a PMOS device is coupled to read bit line and read word line, and an NMOS device is coupled to write bit line. However, Atwood et al. discloses a DRAM cell (Figure 3, MC) can substitute NMOS device is PMOS or PMOS can be NMOS (Column 8, lines 28-39). See Office Action, page 4, last paragraph.

Applicants respectfully submit that the teachings of *Atwood* are not combinable with the teaching of either *Van der Wagt* or *Yoshimoto*. The Examiner appears to have cited *Atwood* for the proposition that an NMOS and a PMOS device are interchangeable in any memory device. However, Applicants submit that such a reading of *Atwood* is clearly wrong. That is, *Atwood* teaches using a p-channel **or** an n-channel device as the storage transistor of a particular **three-transistor memory cell having a particular structure** that is distinct from the structure as recited in claim 1. See Figure 3, col. 8, lines 28-39 of *Atwood*. Applicants submit that such teachings, as they relate to a **three-transistor memory cell** having a particular structure, are not applicable to the teachings of *Van der Wagt* or *Yoshimoto*, which relate to two-transistor

memory cells. For at least this reason, Applicants submit that claim 11 is patentable over *Van der Wagt*, *Yoshimoto*, and in further view of *Atwood*.

Claims 12-17 depend from and add additional features to claim 11. Therefore, by virtue of their dependency, claims 12-17 are also patentable over *Van der Wagt*, *Yoshimoto*, and in further view of *Atwood*.

CONCLUSION

In view of the foregoing, the Applicants respectfully submit that claims 1-3, 11-17 and 21-23 are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at (503) 796-2099.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 10/10/05

James J. Namiki
Registration No. 51,148

Pacwest Center, Suite 1900
1211 SW Fifth Avenue
Portland, Oregon 97204
Telephone: 503-222-9981